10/033114 Complete Set of Claims

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

CLAIMS LISTING (all of pending claims 1-58)

1. (*Currently Amended*) A method of depositing silicon dioxide into trenches defined in a semiconductor substrate, where at least two of the trenches are of different aspect ratios, said depositing method comprising:

(a) using oxygen and silane gases to reactively form silicon dioxide for deposition into said different trenches of the substrate;

(b) using ions to sputter etch a portion of the formed silicon dioxide during the deposition so as to fill the trenches with the formed silicon dioxide without creating voids of substantial size during said filling of said different trenches; and

(c) controlling the etch and the deposition of the silicon dioxide such that a nonzero etch to deposition ratio of about 0.07 or less is established during the filling of said different trenches.

2. (*Original*) The method of Claim 1 further comprising controlling the deposition and the etch such that the etch to deposition ratio is 0.025 or less.

3. (*Original*) The method of Claim 1 further comprising using an oxygen to silane ratio of 1.3 or less.

4. (*Original*) The method of claim 1 further comprising using a total gas flow of the oxygen, the silane, and an inert gas of 625 standard cubic centimeters per minute or less.

5. (*Original*) The method of Claim 1 further comprising using a total gas flow of the oxygen, the silane, and an inert gas of 500 standard cubic centimeters per minute or less.

6. (Original) The method of Claim 1 further comprising using a high frequency bias signal power of 2000 watts or less.

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7. (Original) The method of Claim 1 further comprising using a high frequency bias signal power of 1500 watts or less.

8. (Original) The method of Claim 1 further comprising the act of doping the silicon dioxide during deposition.

9. (Original) The method of Claim 1 further comprising the act of depositing the silicon dioxide over an electrically conductive layer used as an interconnect.

10. (Original) The method of Claim 9, wherein the electrically conductive layer is metal.

11. *(Previously presented)* A method of depositing silicon dioxide over a semiconductor substrate, comprising:

using oxygen and silane gases to deposit silicon dioxide over the substrate;

using ions to etch a portion of the deposited silicon dioxide during the deposition;

controlling the etch and the deposition of the silicon dioxide such that an etch to deposition ratio is 0.07 or less

depositing the silicon dioxide over a layer of silicon nitride, the silicon nitride being formed over a layer of polycrystalline silicon;

polishing the silicon dioxide to expose a top surface of the silicon nitride; and

etching the silicon dioxide such that a top surface of the etched silicon dioxide is below a top surface of the layer of polycrystalline silicon.

12. *(Currently Amended)* An integrated circuit structure comprising silicon dioxide filling at least two trenches of differing widths, where the trench-filling silicon dioxide of said at least two trenches is the product of a method comprising:

(a) using oxygen and silane gases to reactively form the silicon dioxide;

(b) using ions to etch a portion of the formed silicon dioxide; and

(c) controlling the etch and the deposition of the silicon dioxide such that a nonzero etch to deposition ratio of about 0.07 or less is established during the filling of said at least two trenches of differing widths, where said filling does not create voids of substantial size in said two trenches of differing widths.

13. (Original) The integrated circuit of Claim 12, wherein the etch to deposition ratio is 0.025 or less.

14. (Original) The integrated circuit of Claim 12, wherein using oxygen and silane gases comprises using an oxygen to silane ratio of 1.3 or less.

15. (Original) The integrated circuit of Claim 12, wherein using oxygen and silane gasses comprises using a total gas flow rate of the oxygen, the silane, and an inert gas, the total gas flow rate being 625 standard cubic centimeters per minute or less.

16. (Original) The integrated circuit of Claim 12, wherein using oxygen and silane gasses comprises using a total gas flow rate of the oxygen, the silane, and an inert gas, the total gas flow rate being 500 standard cubic centimeters per minute or less.

17. (*Previously presented*) The integrated circuit of Claim 12, wherein the ions used during deposition of the silicon dioxide are subjected to a high frequency bias signal power of 2000 watts or less.

18. *(Previously presented)* The integrated circuit of Claim 12, wherein the ions used during deposition of the silicon dioxide are subjected to a high frequency bias signal power of 1500 watts or less.

19. *(Previously presented)* A method of depositing silicon dioxide into trenches defined in a semiconductor substrate, where at least two of the trenches are of different aspect ratios, said depositing method comprising:

(a) using silane gas, oxygen gas, and an inert gas to reactively form, deposit, and resputter the silicon dioxide, wherein a ratio of oxygen inflow rate to silane inflow rate is 1.7 or less, and wherein the total flow rate of the silane, oxygen, and inert gasses is 500 standard cubic centimeters per minute or more; and

(b) controlling a bias signal which affects a sputter etch action of the inert gas to thereby establish an etch-to-deposition ratio for the formed silicon dioxide which is less than 0.075 .

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20. *(Previously presented)* The method of Claim 19, wherein the ratio of oxygen to silane inflow rates is 1.3 or less.

21. *(Previously presented)* The method of Claim 19, wherein the bias signal is controlled to have a power of 2000 watts or less.

22. *(Previously presented)* The method of Claim 19, wherein the bias signal is controlled to have a power of 1500 watts or less.

23. *(Previously presented)* The method of Claim 19, wherein a total flow rate of the silane, oxygen, and inert gasses is 625 standard cubic centimeters per minute or less.

24. *(Previously presented)* An integrated circuit structure comprising silicon dioxide formed in plural trenches where at least a first trench is at least twice as wide a second of the trenches, the silicon dioxide having been deposited by a deposition method comprising:

(a) using silane gas, oxygen gas, and an inert gas to reactively form, deposit, and resputter the silicon dioxide, wherein a ratio of oxygen inflow rate to silane inflow rate is 1.7 or less, and wherein the total flow rate of the silane, oxygen, and inert gasses is 500 standard cubic centimeters per minute or more; and

(b) controlling a bias signal which affects a sputter etch action of the inert gas to thereby establish an etch-to-deposition ratio for the formed silicon dioxide which is less than 0.075 .

25. *(Previously presented)* The integrated circuit of Claim 24, wherein the ratio of oxygen to silane inflow rates is 1.3 or less.

26. (Original) The integrated circuit of Claim 24, wherein the signal has a power of 2000 watts or less.

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27. (Original) The integrated circuit of Claim 24, wherein the signal has a power of 1500 watts or less.

28. *(Previously presented)* The integrated circuit of Claim 24, wherein a total flow rate of the silane, oxygen, and inert gasses is 625 standard cubic centimeters per minute or less.

29. *(Previously presented)* A method of depositing silicon dioxide into trenches defined in a semiconductor substrate, where at least two of the trenches are of different aspect ratios, said depositing method comprising:

(a) using silane gas, oxygen gas, and helium gas to reactively form, deposit, and resputter the silicon dioxide, wherein a ratio of oxygen inflow rate to silane inflow rate is 1.7 or less; and

(b) controlling a bias signal which affects a sputter etch action of the helium gas to thereby establish an etch-to-deposition ratio for the formed silicon dioxide which is less than 0.075 .

30. *(Previously presented)* The method of Claim 29, wherein the ratio of oxygen to silane inflow rates is 1.3 or less.

31. (Original) The method of Claim 29, wherein the signal has a power of 2000 watts or less.

32. (Original) The method of claim 29, wherein the signal has a power of 1500 watts or less.

33. (Original) The method of claim 29, wherein a total flow rate of the silane, oxygen, and helium gasses is 625 standard cubic centimeters per minute or less.

34. (Original) The method of claim 29, wherein the total flow rate is 500 standard cubic centimeters per minute or less.

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35. *(Previously presented)* An integrated circuit structure comprising silicon dioxide formed in plural trenches where at least a first trench is at least twice as wide a second of the trenches, the silicon dioxide having been deposited by a deposition method comprising:

(a) using silane gas, oxygen gas, and a helium gas to reactively form, deposit, and resputter the silicon dioxide, wherein a ratio of oxygen inflow rate to silane inflow rate is 1.7 or less; and

(b) controlling a bias signal which affects a sputter etch action of the helium gas to thereby establish an etch-to-deposition ratio for the formed silicon dioxide which is less than 0.075.

36. *(Previously presented)* The method of Claim 35, wherein the ratio of oxygen to silane inflow rates is 1.3 or less.

37. (Original) The method of Claim 35, wherein the signal has a power of 2000 watts or less.

38. (Original) The method of Claim 35, wherein the signal has a power of 1500 watts or less.

39. (Original) The method of Claim 35, wherein a total flow rate of the silane, oxygen, and helium gasses is 625 standard cubic centimeters per minute or less.

40. (Original) The method of Claim 35, wherein the total flow rate is 500 standard cubic centimeters per minute or less.

41. *(Previously presented)* The depositing method of Claim 1 wherein a first of said trenches is at least twice as wide as a second of said trenches.

42. *(Previously presented)* The depositing method of Claim 1 wherein a first of said trenches has a width in the range of about 1800Å to 3300Å and a second of said trenches has a width in the range of about 6600Å to 8800Å.

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43. *(Previously presented)* The method of Claim 1 and further comprising:

(d) overfilling said at least two of the trenches with the deposited silicon dioxide; and

(e) using chemical mechanical polishing (CMP) to remove at least a portion of the overfilling silicon dioxide.

44. *(Previously presented)* The method of Claim 43 and further wherein said at least two of the trenches have silicon nitride at top portions thereof and said CMP removal stops at the silicon nitride top portions of said at least two trenches.

45. *(Previously presented)* The method of Claim 1 wherein the used ions include helium.

46. *(Previously presented)* A method of using high-density plasma chemical-vapor deposition (HDP-CVD) to deposit silicon oxide on a semiconductor-containing substrate having trenches defined therein, where the trenches include those of different aspect ratios, at least one trench having a relatively high depth-to-width aspect ratio equal to or greater than 2.5 and at least a second trench having a depth-to-width aspect ratio which is comparatively smaller, said HDP-CVD method comprising:

(a) applying one or more electromagnetic fields to an ionized plasma containing oxygen, silane, and an inert gas where the oxygen and silane of the plasma can reactively combine to form first silicon oxide for deposition on the semiconductor-containing substrate; and

(b) controlling at least one of:

(b.1) the oxygen-to-silane ratio in the plasma,

(b.2) a first of the electromagnetic fields, and

(b.3) total input gas flow for supplying said oxygen, silane, and inert gas to said plasma,

to thereby establish a nonzero etch-to-deposition ratio (E/D ratio) condition of about 0.07 or less where said E/D ratio can be defined as a difference in thickness of net deposited silicon oxide with said first electromagnetic field turned on and off divided by the thickness of net deposited silicon oxide with said first electromagnetic field turned off.

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47. *(Previously presented)* The HDP-CVD method of Claim 46 wherein the ionized plasma further contains a sputter etch agent which can sputter etch at least a portion of the deposited first silicon oxide; and

(b.3a) the total gas inflow of the oxygen, silane and the sputter etch agent is about 625 standard cubic centimeters per minute (sccm) or less.

48. *(Previously presented)* The HDP-CVD method of Claim 46 wherein the first silicon oxide includes silicon dioxide.

49. *(Previously presented)* The HDP-CVD method of Claim 46 wherein the first silicon oxide includes phospahate silica glass.

50. *(Previously presented)* The HDP-CVD method of Claim 46 wherein the comparatively smaller aspect ratio of the second trench less than about 1.

51. *(Previously presented)* The HDP-CVD method of Claim 50 wherein the first trench has a width in the range of about 1800Å to 3300Å.

52. *(Previously presented)* The HDP-CVD method of Claim 46 wherein the inert gas includes helium.

53. *(Currently amended)* A monolithically integrated device having a semiconductor-containing substrate and plural trenches defined to extend into at least one layer of the device to substantially same depths, where at least a first and second of said same-depth trenches respectively have different widths, the width of the second trench being at least twice the width of the first trench, said integrated device being further characterized by:

(a) said same depth trenches of different widths are each filled with a silicon oxide deposited by way of high-density plasma chemical-vapor deposition (HDP-CVD) to substantially same heights above said substantially same depths to thereby provide a substantially planar set oxide-filled trenches upon which other layers of material are founded where said oxide-filled trenches do not have voids of substantial size defined therein.

54. *(Previously presented)* The integrated device of Claim 53 wherein:

(b) the heights of said oxide-filled trenches lie adjacent to silicon regions.

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55. *(Previously presented)* The integrated device of Claim 54 wherein:

(b.1) the heights of said oxide-filled trenches are within about 600Å of reference top surfaces of the adjacent to silicon regions.

56. *(Previously presented)* The integrated device of Claim 54 wherein:

(b.1) the heights of said oxide-filled trenches are defined at least by chemical mechanical polishing (CMP).

57. *(Previously presented)* The integrated device of Claim 56 wherein:

(b.2) the heights of said oxide-filled trenches are further defined by an acid etch carried out after said chemical mechanical polishing (CMP).

58. *(Previously presented)* The integrated device of Claim 57 wherein:

(b.3) the heights of said oxide-filled trenches, after said acid etch, are within about 600Å of reference top surfaces of the adjacent to silicon regions.

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